

Figure 1 Architecture of A Multi-Stage Multi-Dimensional Switch to which the claimed technique is applied (usually $N > M$)

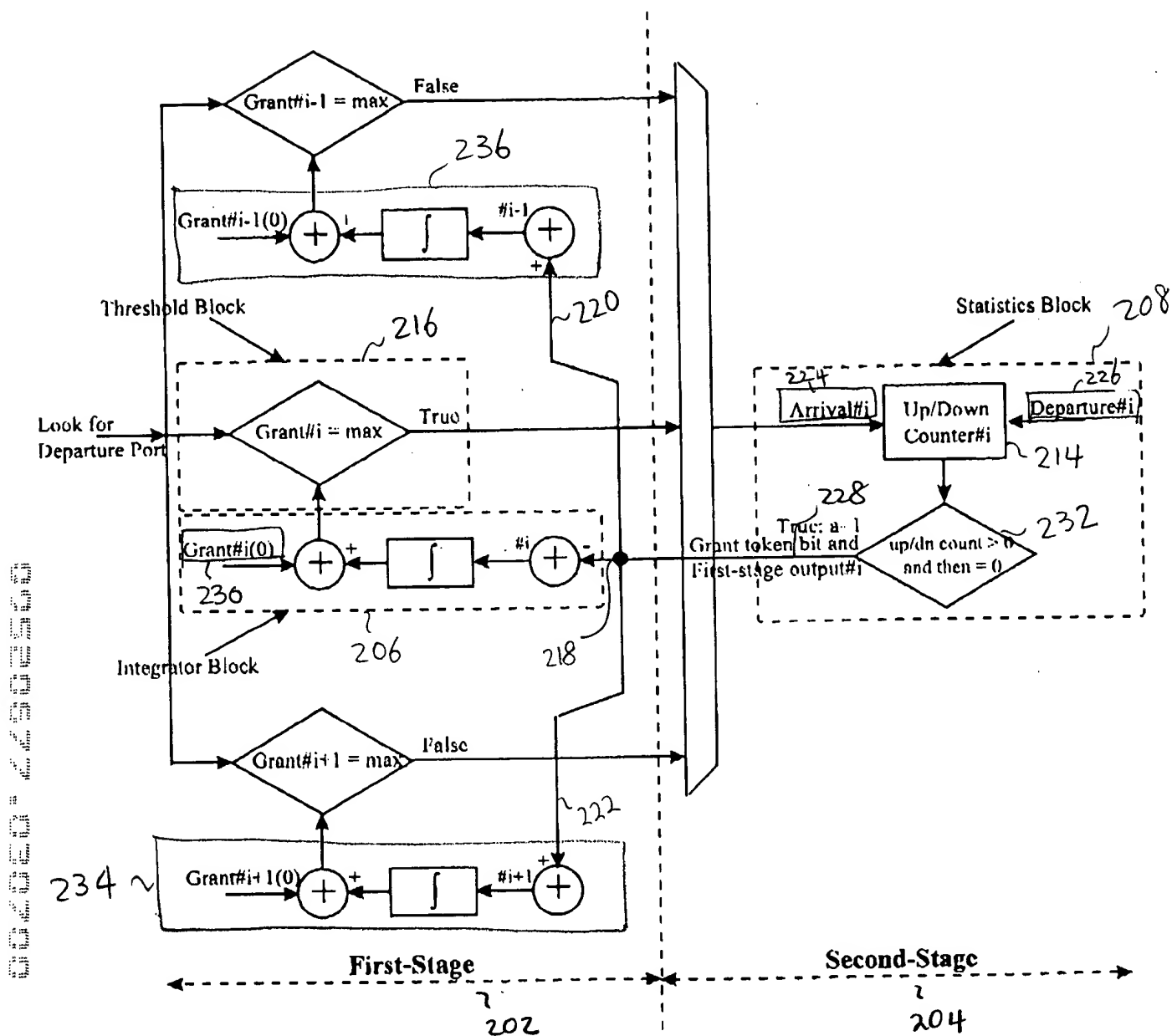


Figure 2 Structure of An Adaptive Credit-Based Flow Control Logic Inside Each Switch Element at First Stage and Inside Each Crossconnect Element at Second Stage When Data Packet Arrives At Second-Stage From Input Port#i of First-Stage

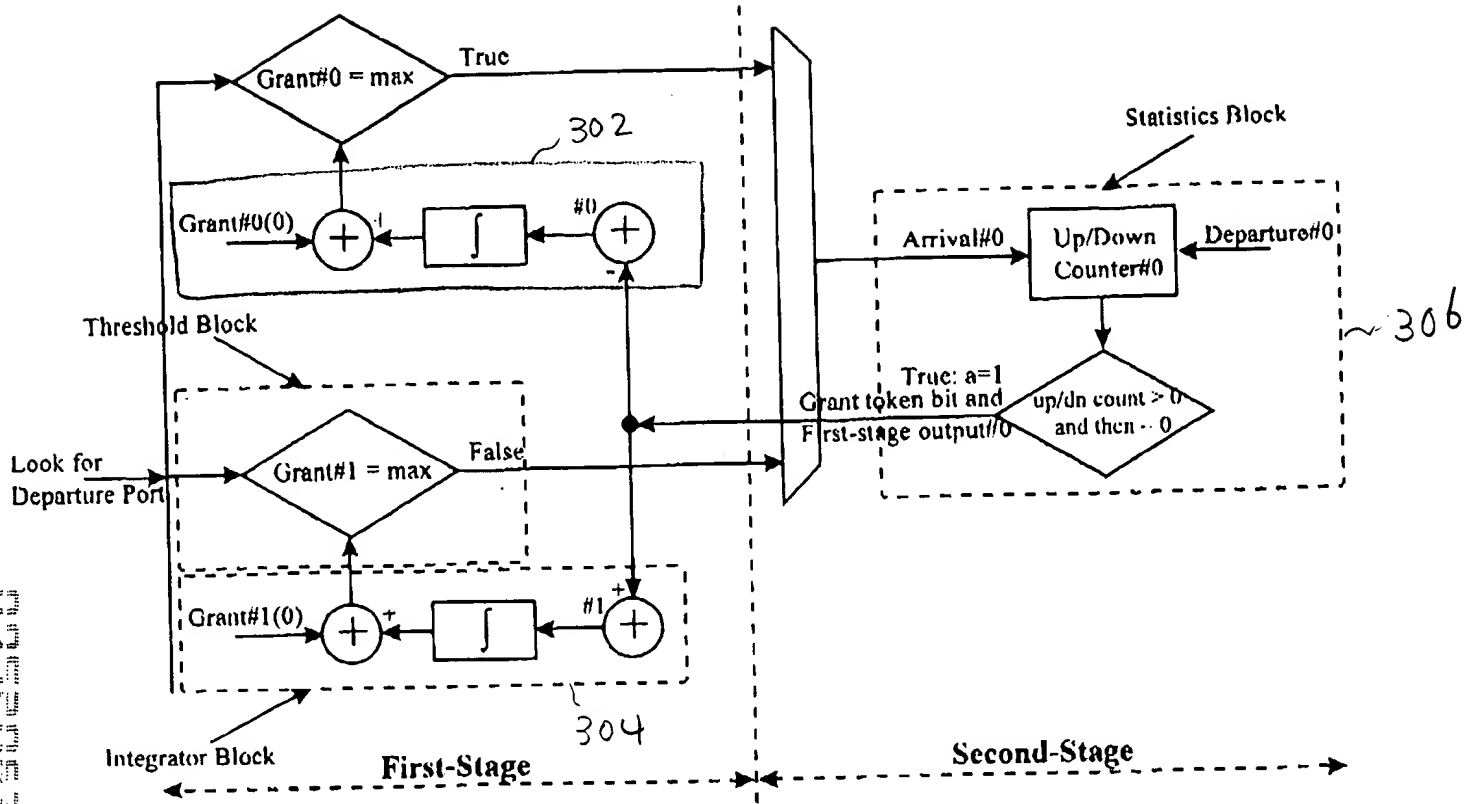


Figure 3 Upper Boundary of An Adaptive Credit-Based Flow Control Logic When Data Packet Arrives at Second-Stage From Output Port#0 of First-Stage

400

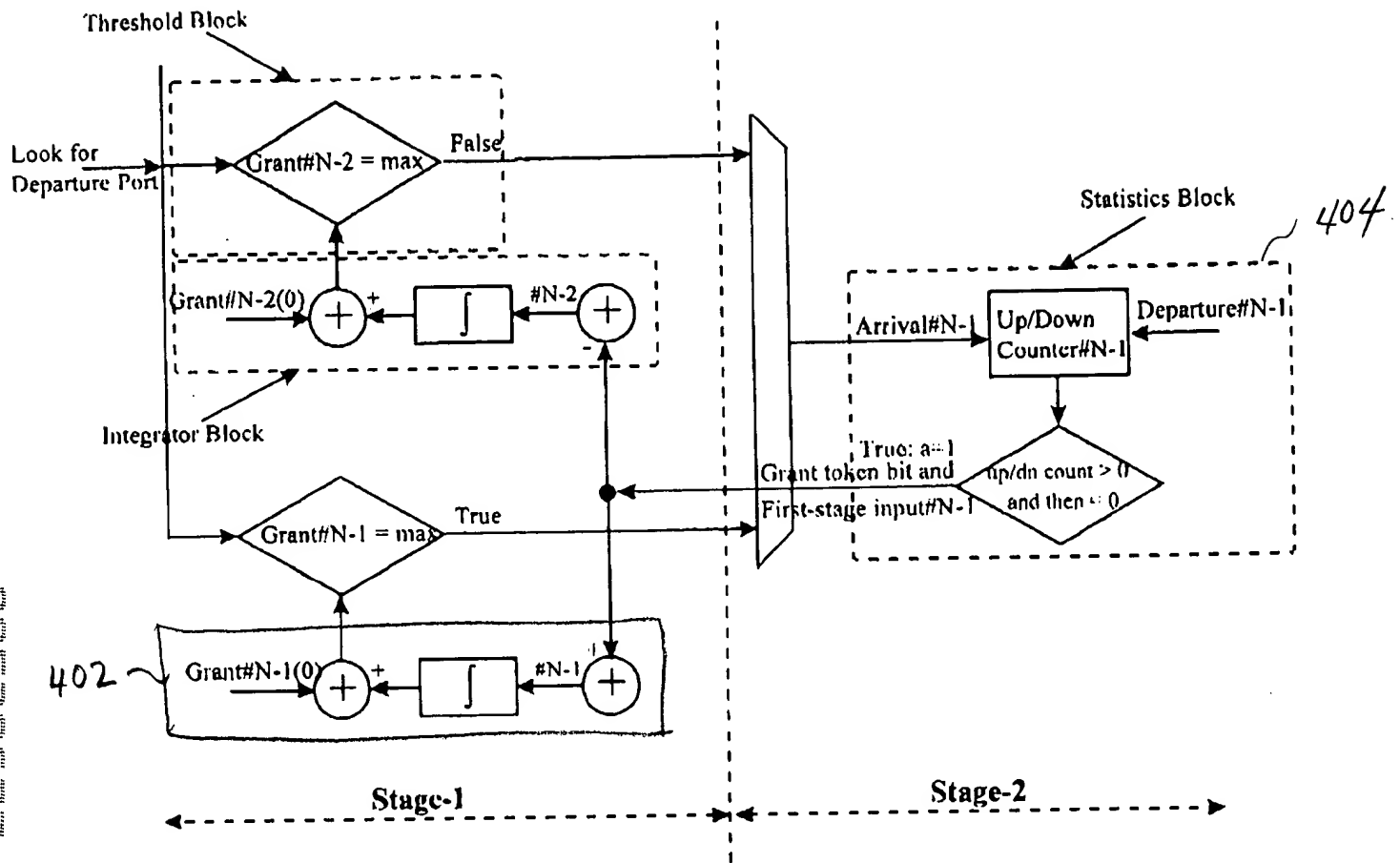


Figure 4 Bottom Boundary of An Adaptive Credit-Based Flow Control Logic When Data Packet Arrives at Second-Stage From Output Port#N-1 of First-Stage

500

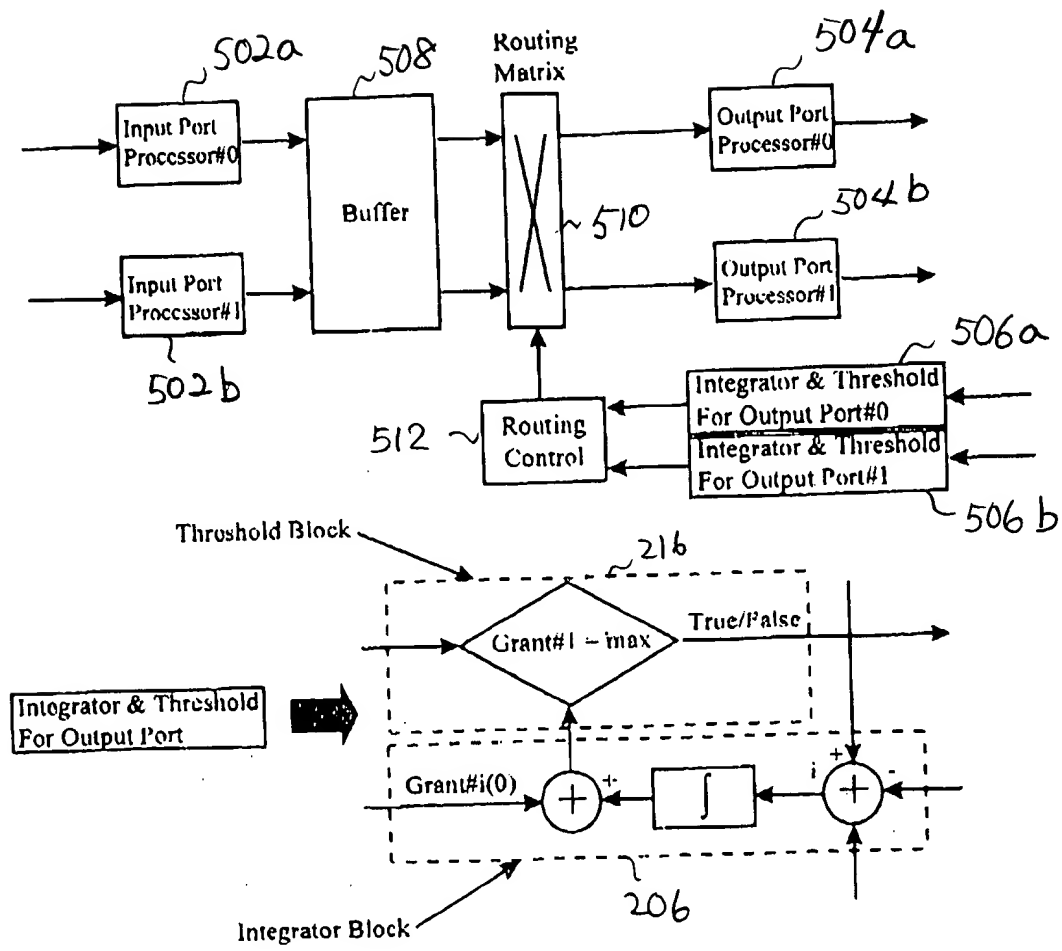


Figure 5 Internal Logic Flow of A Two-Port First-Stage Switch Element As Example

5600

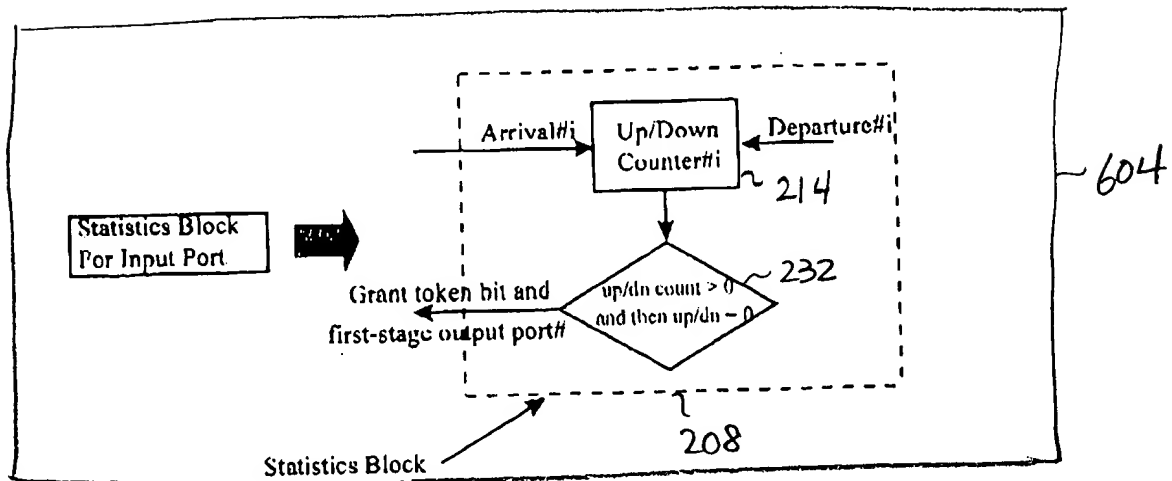
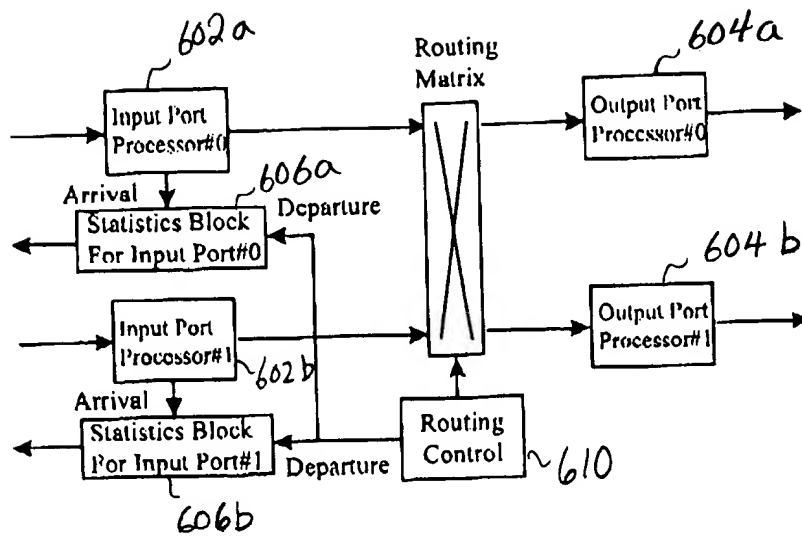


Figure 6 Internal Logic Flow of A Two-Port Second-Stage Crossconnect Element As Example